

CSE 2312-001

Practice Exam 1

Practice A

ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Multiple Choices (50 points total / 2 points each)

1. What is the order of the process of manufacturing from Silicon to IC?
2. Silicon ingot, Dicer, Tested dies, Bond die to package, Packaged dies, Part tester, Tested packaged dies, Slicer, Blank wafers, 20 to 40 processing steps, Patterned wafers, Wafer tester, Tested Wafer, Ship to customers.
3. Silicon ingot, 20 to 40 processing steps, Patterned wafers, Slicer, Blank wafers, Wafer tester, Tested wafer, Dicer, Tested dies, Part tester, Tested packaged dies, Bond die to package, Packaged dies, Ship to customers.
4. Silicon ingot, Part tester, Tested packaged dies, Bond die to package, Packaged dies, Dicer, Tested dies, Wafer tester, Tested wafer, 20 to 40 processing steps, Patterned wafers, Slicer, Blank wafers, Ship to customers.
5. Silicon ingot, Slicer, Blank wafers, 20 to 40 processing steps, Patterned wafers, Wafer tester, Tested wafer, Dicer, Tested dies, Bond die to package, Packaged dies, Part tester, Tested packaged dies, Ship to Customers.
6. How is cost/performance improving?
7. Based on energy efficiency
8. Due to underlying technology development
9. Use parallelism to improve performance
10. Based on Moore’s Law
11. What affects performance of a program?
12. Algorithm, Programming Language, Compiler, Instruction set architecture
13. Algorithm, Assembler, Compiler, Instruction set architecture
14. Programming Language, Assembler, Compiler, Instruction set architecture
15. Algorithm, Programming Language, Assembler, Instruction set architecture
16. Which is NOT RISC architecture?
17. SPARC
18. Power
19. MIPS
20. Core
21. What is a word?
22. A given instruction
23. A data variable
24. A registry data
25. A group of 32 bits
26. A group of 16 bits
27. Which storage can be accessed the fastest?
28. Dynamic RAM (DRAM)
29. Static RAM (SRAM)
30. Magnetic disk
31. Any of the above can be accessed the fastest
32. How are negative binary numbers represented?
33. Unsigned Binary Integers
34. The Zero Constant
35. 2s-complement Signed Integers
36. Sign Extension
37. What does a bitwise shift left do?
38. It shifts the bits in the binary number to the left
39. It shifts the integers to the left of the equation
40. It shifts the integers to the left of the register
41. It shifts the rightmost bit to the left.
42. How does a stack pointer and a frame pointer work when each register is saved or restored?
43. A stack pointer is fixed on the register base, a frame pointer changes
44. A stack pointer changes, a frame pointer is fixed on the register base
45. A stack pointer is fixed on the register base, a frame pointer is fixed on the register base
46. A stack pointer changes, a frame pointer changes
47. What is the process to start a program?
48. compiler -> assembler -> linker -> loader
49. loader -> compiler -> linker -> assembler
50. compiler -> linker -> loader -> assembler
51. loader -> linker -> compiler -> assembler
52. linker -> compiler -> assembler -> loader
53. How many registers are in MIPS?
54. 8
55. 16
56. 32
57. 64
58. Which instructions modify registers?
59. R-type
60. J-type
61. I-type
62. None of the above

How to fix pipeline hazards?

1. Which of the following is not an advantage of a write-back?
2. Individual words can be written by the processor at the rate that the cache, rather than the memory, can accept them.
3. Multiple writes within a block require only one write to the lower level in the hierarchy.
4. When blocks are written back, the system can make effective use of a high-bandwidth transfer, since the entire block is written.
5. Write-back is easier to implement than write-through, although to be practical, a write-back cache will still need to use a write buffer.
6. Which of the following is not an advantage of a write-through?
7. Misses are simpler and cheaper because they never require a block to be written back to the lower level.
8. Multiple writes within a block require only one write to the lower level in the hierarchy.
9. Write-through is easier to implement than write-back, although to be practical, a write-through cache will still need to use a write buffer.
10. None of the above
11. A computer writes random values continuously to a single block of memory on a flash disk for an indefinite amount of time. Which failure is most likely to occur?
12. The drive overheats
13. The drive capacity is exceeded
14. Some bits on the drive fail to change values
15. The drive seek time increases
16. The drive RPM decreases
17. How is memory stored in DRAM?
18. It is stored as a charge on the capacitor
19. It is stored as a magnetic direction on the cell
20. It is stored as a sensitive bit.
21. It is stored as a temporary bit.
22. What is the order of the pipeline guidelines?
23. WB, MEM, EX, ID, IF
24. WB, MEM, EX, IF, ID
25. ID, IF, WB, WB, MEM
26. IF, ID, EX, MEM, WB
27. What is the number of OpCodes MIPS can support?
28. 64
29. 128
30. 256
31. 512

Free Response (50 points total)

1. Consider three processors (P1, P2, P3), each with the same instruction set. P1 has a 1.5 GHz clock rate and a CPI of 2.0. P2 has a 2.0 GHz clock rate and a CPI of 2.5. P3 has a 2.5 GHz clock rate and a CPI of 4.0.
2. Compute the instructions per second for each processor.
3. For each processor executing a different program in 10 seconds, compute the number of cycles and the number of instructions that were performed.
4. For each processor executing the programs in part b, the CPI is increased by 20%. We now wish to reduce
5. Consider 2 processors (P1 and P2). P1 has a clock rate of 2.5 GHz, a voltage of 1.25 V, and a dynamic power expenditure of 85 Watts. P2 has a clock rate 3.5 GHz, a voltage of 1.0 V, and a dynamic power expenditure of 80 Watts.
6. What is the capacitive load for each processor?
7. Suppose we are able to lower the capacitive load of both processors by 20%, while also decreasing the voltage by 15%. What is the affect on dynamic power for each processor?
8. Assume a 20 cm diameter wafer has a cost of $500, contains 80 dies, and has 0.04 defects/cm2.
9. Compute the yield for this wafer.
10. Compute the cost per die for this wafer.
11. If the number of dies per wafer is increased by 10%

3. Translate the following MIPS code into C. Let integers x, y, and z be stored in $a0, $a1, and $a2, respectively.

fun: add $t0, $a0, $a1

sub $t0, $t0, $a2

add $v0, $t0, $zero

jr $ra



1. Consider the single stage CPU represented in the diagram. Complete the control line table below for the given instructions by entering 0, 1, or x for “don't care”.

Instruction #1: sltu $t0,$t1,$t2

Instruction #2: 10101100011000100000000000010100

Instruction #3: sh $t0,$t1,100

Instruction #4: beq $t0,$t1,L1

Instruction #5: 0x0B090001

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | RegDst | Branch | MemRead | MemtoReg | MemWrite | ALUSrc | RegWrite |
| #1 |  |  |  |  |  |  |  |
| #2 |  |  |  |  |  |  |  |
| #3 |  |  |  |  |  |  |  |
| #4 |  |  |  |  |  |  |  |
| #5 |  |  |  |  |  |  |  |

1. Compute the average read time for a *Seagate Barracuda ST750DM003* hard drive using the attached manufacturer product specification. Use the listed value for *average latency* in place of *average seek time* in your calculations, and a sector size of 512 bytes (the specification lists 4096 byte sectors, but these are emulated as 512 byte sectors to the OS). Also use the listed value for *average data rate* in place of *transfer rate*, and assume the 0.1ms of controller overhead.
2. The table below represents the same scenario as part 2 using a write-back cache...

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Index** | **V** | **Tag** | **Data** | **Dirty** |
| 000 | Y | 01 | Mem[01000] | N |
| 001 | N |  |  | N |
| 010 | Y | 10 | Mem[10010] | N |
| 011 | N |  |  | N |
| 100 | N |  |  | N |
| 101 | N |  |  | N |
| 110 | Y | 11 | Mem[11110] | N |
| 111 | Y | 00 | Mem[00111] | N |

a) Show the modified table after the following the following sequence of cache accesses (listed by address): {0x1F, 0x1D, 0x12, 0x1B, 0x1E}. Assume that underlined accesses correspond to cache writes, while all others correspond to cache reads.

b) Which of the accesses from part 3a result in a read hit?

c) Which of the accesses from part 3a will immediately change a value in memory?